Total Impact briQ.

Hardware Reference

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Revision 0.4

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1   Overview

2   On-board Peripherals

2.1   CPU/L2 Cache

The briQ uses intersposer technology for the CPU, L2 cache combo. This technology mounts the CPU and the L2 cache on a separate daughtercard that is socketed onto the main board. This allows for relatively easy upgrades of the CPU on the main board.

Currently the briQ features PowerPC 750 and 7400 CPU's at speed's of up to 500MHz. The L2 cache is available in pipelined configurations in CPU/L2 bus speed ratios of 3:1, 5:2 and 2:1, in both 0.5MB and 1Mb sizes. There is also a late-write L2 cache option of 1Mb at an L2 bus ratio of 3:2.

2.2   PPC/PCI Bridge

The briQ features the IBM CPC710 as the main bridge chip between the CPU and the rest of the system hardware. The CPC710 provides the 100MHz SDRAM interface as well as two PCI bridges, one 32 bit 33MHz, and on 64 bit, 66 MHz. The CPC710 is a complex device, information on programming the CPC710 can be obtained from the CPC710-100+ User Manual, available at http://www.fr.ibm.com/france/cdlab/avi.htm.

2.3   SDRAM

The briQ has two standard 168 pin DIMM sockets on board. These sockets should be populated with standard PC100 Synchronous DRAM. Both sockets must be populated in order for the briQ to function correctly, and both sockets must be populated with identical DIMM's.

Current technology allows up to 512MB per DIMM socket, so the briQ is capable of having up to 1GB of SDRAM memory on board.

2.4 Flash Memory - AMD 29LV081B

The briQ features 1MB of on-board executable flash memory which supports direct code execution.

2.5 Ethernet Interface - AMD 79C973

The Am79C973 ethernet controller provides a 10/100BaseT interface on the briQ. The briQ is connected to an ethernet network using a standard RJ-45 connector at the back of the case. Detection of a 10Mbit or 100Mbit connection is automatic.

Four LED's are present on the briQ to provide information about the status of the ethernet link. These LED's are located at the top of the board and are not visible externally. The meaning of each of these LED's is:

op Lit when a 100Mbit connection is detected

Tx Lit when the briQ is transmitting data

Ac Lit when a valid ethernet link is detected

Rx Lit when the briQ is receiving data.

The Am79C973 is connected via the 32 bit PCI bus as device #7, and contains the standard PCI configuration registers along with some device specific configuration registers. In addition the Am79C973 has other operational registers which are accessible through the PCI I/O space on the PCI32 bus.

By default on the briQ the Am79C973 is configured by the SmartFirmWare(tm) to use IRQ12 (INTD) at boot time.

More information on the Am79C973 can be found by referring to the Am79C973/Am79C975 PCnet(tm)-FAST III datasheet.

The file drivers/net/pcnet32.c in the linux source code is a good source of information about programming the Am79C973.

2.6 PCI/ISA Bridge - Winbond W83C553F

The Winbond W83C553F integrates the functionality of PCI Bus master IDE controller, PCI arbiter, two 82C37A DMA controllers, two 82C59 programmable interrupt controllers, a 82C54 counter/timer.

The W83C553 acts as a bridge between the 32 bit PCI and ISA expansion bus on the briQ, mapping the ISA I/O space to the bottom of the PCI I/O space, making the ISA peripheral registers easily accessible via the 32 bit PCI bus I/O space. The W83C553 also routes PCI interrupts to ISA interrupts.

The W83C553 is connected to the 32 PCI bus of the briQ as device #6. It provides two PCI functions, function 0 being the PCI-ISA bridge, and function 1 being the IDE controller. Both functions provide several device specific configuration registers as well as the standard PCI configuration registers in the PCI configuration space.

Further information on the W83C553 can be found by referring to the W83C553F System I/O controller with PCI Arbiter Data Book, Winbond Electronics Corp, Publication number 2565, Version A.7.0d.

2.7   IDE Interface - Winbond W83C553F

The briQ provides support for up to two IDE devices on a single IDE channel using PCI function 1 of the W83C553F. The IDE interface is fully compliant with the ATA Revision 3.0 and ATA-2 specifications, and each connected device is individually programmable to support ATA defined PIO modes 0-4 and Ultra 33 DMA modes 0-2.

The IDE interface is routed to a connector on the edge of the briQ providing a standard 44 pin notebook (2 mm pitch) IDE connector (J4) for easy attachment to notebook IDE drives.

2.8   Timers/Counters - Winbond W83C553F

The W83C553F includes the equivalent of an 82C54 counter/timer as part of PCI function 0. This section of the device is programmable through the PCI configuration space and also through several standard configuration registers available in the 32 bit PCI bus I/O space.

Three counter/timer channels are provided, connected to an external 14.31818MHz clock through a divide-by-twelve counter. Timers 0 and 1 are always enabled. and timer 2 can be enabled and disabled by programming the appropriate register (port B) in the PCI I/O space.

Timer 0 is connected to IRQ0 of the interrupt controller and timer 2 is connected to the speaker output header (J23) on the briQ.

The W83C553 also contains an additional BIOS Timer which by default decrements at 8.33MHz and is also accessible through the PCI I/O space.

Additional information on programming the W83C553F can be found in the W83C553F System I/O controller with PCI Arbiter Data Book, Winbond Electronics Corp, Publication number 2565, Version A.7.0d.

Other timers/counters available on the briQ include the decrementer register in the CPU and the real time clock.

2.9   Interrupt Controller - Winbond W83C553F

The W83C553F contains the equivalent of two cascaded 82C59 interrupt controllers, and also provides the ability to internally route the four PCI interrupts (INTA - INTD) to an ISA interrupt. The W83C553F also internally routes the IDE interrupt.

The interrupt routing for the briQ is determined by the hardware configuration and also by the values of the interrupt routing control registers in the W83C553. These registers are configured by the firmware at boot time and generally should not need to be altered. The PCI interrupt allocation is shown in table 1.

Interrupt	Default Allocation
INTA	Daughter-board interrupt 1
INTB	Daughter-board interrupt 2
INTC	Daughter-board interrupt 3
INTD	On-board 10/100 BaseT Network Controller Interrupt

Table 1: PCI Interrupt Allocation

and the ISA interrupt allocation is shown in table 2.

Interrupt	Default Allocation
IRQ0	Timer Interrupt
IRQ1	Unused (Keyboard)
IRQ2	Reserved (Cascade)
IRQ3	Unused
IRQ4	UART
IRQ5	INTC (Daughter-board interrupt 3
IRQ6	Unused
IRQ7	Front Panel Switches
IRQ8	Real Time Clock
IRQ9	CPC710 System Interrupt 1
IRQ10	INTA (Daughter-board interrupt 1)
IRQ11	INTB (Daughter-board interrupt 2)
IRQ12	INTD (On-board network interrupt)
IRQ13	Unused (DMA)
IRQ14	IDE Controller Interrupt
IRQ15	CPC710 System Interrupt 2 (DMA Complete)

Table 2: ISA Interrupt Allocation

The PCI (INTA-INTD) interrupts are all level sensitive interrupts allowing them to be shared by several devices. The ISA interrupts (IRQ0-IRQ15) can be programmed to be edge or level sensitive interrupts by programming the Interrupt Edge/Level Control

register in the PCI I/O space. By default these interrupts are configured to be edge sensitive.

2.10   Serial Port - 16C550

The briQ contains a single 16C550 compatible Universal Asynchronous Receiver Transmitter (UART). This communications port is routed to a standard 9 pin DIN connector (J2) at the back of the briQ.

The 16C550 is attached via the ISA peripheral bus, with the control registers being available in the ISA I/O space, which is in turn mapped to the bottom of the 32 bit PCI bus I/O space. The control registers are located at a fixed memory address 0x3F8-0x3FF. The 16C550 is connected to IRQ4.

Additional information on programming the 16C550 can be found in the Texas Instruments Data Sheet for the TL16C550C, TL16C550CI Asynchronous Communications Element with Autoflow Control (SLLS177E)

2.11   NVRAM - DS 17285S

The DS 17285S is used by on the briQ to provide 2k + 114 bytes of battery backed, non-volatile SRAM. This NVRAM is used by the SmartFirmWare(tm) to store boot time parameters and incorrect usage may render the briQ inoperable, requiring it to be returned to the manufacturer. As such the NVRAM is not recommended for general use.

The DS17285S is an ISA peripheral mapped to the ISA I/O space at addresses 0x070-0x077. The even addresses within this range are used to set the register within the DS17285 that is to be written, and the odd addresses are used to read and write data to the selected register. These addresses are mapped in the 32 bit PCI bus I/O space.

The NVRAM can be write protected by removing jumper JP4.

Additional information of programming the NVRAM can be found in the Dallas Semiconductor Data Sheet for the DS17285/DS17287.

2.12   Real Time Clock - DS 17285S

The DS17285S provides the briQ with a battery backed Y2K compliant real time clock and calendar, with automatic leap year compensation, automatic daylight savings adjustment and a date alarm function.

The real time clock registers are accessed through the same ISA I/O addresses as the NVRAM, with offset 0x070 setting the register address, and 0x071 reading/writing data.

Writes to the real time clock are disabled by removing jumper JP4.

Information on programming the DS17285 can be found in the DS17285/DS17287 Data Sheet available from Dallas Semiconductor.

2.13   Watchdog Timer - LTC1232

The LTC1232 provides power supply monitoring, reset and watch dog timer facilities for the briQ.

When the briQ is powered up the watch dog timer is disabled. The watch dog timer is armed by writing a 1 to bit 0 (0x01) of ISA I/O address 0x3E0. Once armed the watch dog timer cannot be disabled and the processor has 1.2 seconds to generate a watch dog timer reset. If a watch dog timer reset is not generated within 1.2 seconds the briQ will be reset.

A watch dog timer reset is generated by first writing a 1, then a 0 to bit 0 of ISA I/O address 0x3E0.

The current state of the watch dog timer can be determined by reading bit 7 of ISA I/O address 0x398. A value of 1 in this bit indicates the watchdog timer is enabled.

2.14   Front Panel Display - Futaba 202-SD-16GN

The front panel of the briQ features a vacuum fluorescent display (VFD) used to display information about the status of the briQ.

This display module is compatible with the standard NA202SD16AA3 LCD emulator and features a two line display, with up to twenty characters capable of being displayed on each line.

The VFD is located at the fixed ISA I/O addresses 0x390-0x39F. Writing a value to even addresses within this range will send a command to the VFD, reading from the even addresses will retrieve a status byte from the display. Writing to the odd addresses within this range will send data to the display, reading the odd addresses will retrieve the current data from the display.

More information on prgramming the VFD can be found in the LCD Emulators document from Futaba Corpoartion of America.

2.15   Front Panel LED

The briQ's front panel also features a tricolor LED located at ISA I/O address 0x398. The color displayed by the LED is controlled by bits 0 and 1 at this location as shown in table 3. These bits can also be read to determine the current color displayed by the LED.

Bit 1	Bit 0	Output Color
0	0	LED Off
0	1	Red
1	0	Green
1	1	Amber

Table 3: Controlling the Front Panel LED

2.16 Front Panel Switches

The current values of the the two switches are also represented in the byte located at address 0x398. Bits three corresponds to the current position of the top switch (labelled with a triangular icon) and bit 4 corresponds to the position of the bottom switch (labelled with a square icon). If the switch is currently depressed then the corresponding bit will contain a value of 0, if the swicth is released the bit will contain a 1.

Both switch inputs are passed through debounce circuitry, and when pressed will generate an interrupt on IRQ7. By default this interrupt is ignored.

2.17 DMA Controller

2.18 64 Bit PCI Bus expansion socket

3 Memory Map

Each of the major sub-systems in the Total Impact briQ is mapped into the physical memory space by various control registers within the CPC710. The configuration is determined by the SmartFirmWare(tm) at boot time. Generally this default configuration should not need to be changed.

Within each major sub-section each individual device is located, some of these devices may also be relocatable within their specific section, although generally this should not be necessary.

Each bridge within the briQ has a varying degree of access to the other bridges in the system, along with it's own memory map. Each of these maps is described in the following sections.

It is also important to note that the addresses specified here are physical addresses. If an operating system that uses a virtual memory management scheme (as linux does) is employed then the addresses seen at the user or operating system level may be different again.

3.1 System Memory Map

The system memory map represents the briQ's hardware components as seen by the CPU. The memory map is determined by the porgramming of the CPC710 Dual Bridge and Memory Controller. The configuration is determined at boot time by the firmware and is arranged in a CHRP compliant manner. The 4GB address space is divided into several major sections as shown in figure 1.

3.2 PCI 32 to System Addressing

3.2.1 ISA Memory Map

Several devices are connected via the ISA bus which is mapped into the PCI32 I/O address space. These devices are accessed by addressing the appropraite offset within the PCI32 I/O space. Generally this is located at address 0x8000 0000.

Offset Address Range	Device
0x20-0x21	PIC1 Control Registers
0x40-0x43	Timer Control Registers
0x61	NMI Status and Control Register
0x70-0x77	RTC/NVRAM Control Registers
0x78-0x7B	BCLK Timer Registers
0x92	Port 92 Register
0xA0 -0xA1	PIC2 Control Registers
0x1F0-0x1F7	IDE Bus Control Registers
0x390-0x397	VFD Registers
0x398-0x39F	briQ Control Registers
0x3E0-0x3E7	Watch Dog Timer Registers
0x3F8-0x3FF	UART
0x4D0	PIC1 Interrupt Edge/Level control register
0x4D1	PIC2 Interrupt Edge/Level control register

Table 4: ISA Device Memory Map

3.3 PCI 64 to System Addressing

```
0xffff ffff
0xff60 0000
                PCI 32 Configuration Space
0xff50 0000
                PCI 64 Configuration Space
0xff40 0000
0xff10 0000
                        Boot Flash
0xff00 0000


0xd000 0000
                    PCI 64 Memory Space
0xc800 0000
                    PCI 32 Memory Space
0xc000 0000


0x9000 0000
                     PCI 64 I/O Space
0x8800 0000
                     PCI 32 I/O Space
0x8000 0000




                        System Memory




0x0000 0000              10
```
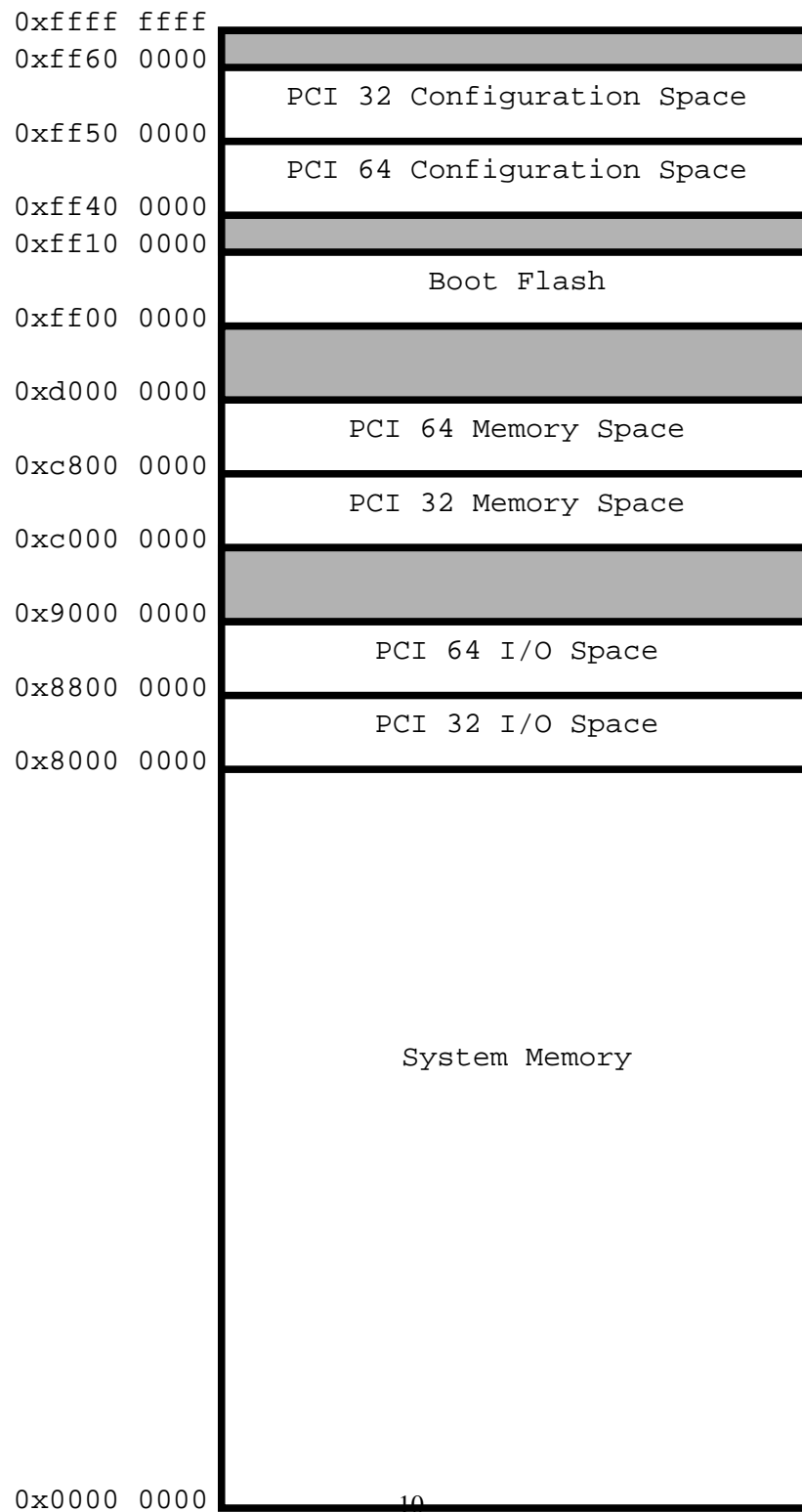
Figure 1: System Memory Map